

In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1 1. (Currently Amended) A method of transferring bursts of
2 data between a processor device and a FIFO device, said transfer
3 comprising:

4 triggering a burst transfer at the processor from ~~the~~ a change
5 of state of a FIFO output signal by the FIFO device, said change of
6 state being ~~the~~ an occurrence of a triggering event within the FIFO
7 device; and

8 inhibiting the FIFO device from changing state of the FIFO
9 output signal thereby inhibiting of triggering of any further burst
10 transfers until a current burst transfer is complete.

1 2. (Original) The method of claim 1, wherein:
2 said triggering event is change in a FIFO fullness indicator
3 flag.

1 3. (Original) The method of claim 2, wherein:
2 said FIFO fullness indicator flag denotes the FIFO is less
3 than or greater than half full; and
4 said triggering event is changing from said FIFO fullness
5 indicator flag denoting less than half full to greater than half
6 full.

1 4. (Original) The method of claim 2, wherein:
2 said fullness indicator denotes less than or greater than half
3 full; and
4 said triggering event is changing from said FIFO fullness
5 indicator flag denoting greater than half full to less than half
6 full.

1 5. (Original) The method of claim 1, wherein:
2 said burst transfer includes transfer of predetermined amount
3 of data in fixed number of sequential clock cycles.

6 to 8. (Cancelled)

1 9. (Currently Amended) The method of claim 1, ~~further~~
2 ~~comprising the step of~~ wherein:
3 said step of inhibiting the FIFO device from changing state of
4 the FIFO output signal, thereby inhibiting further burst transfers
5 includes further inhibiting the FIFO device from changing state of
6 the FIFO output signal until a predetermined number of clock cycles
7 following completion of current burst transfer.

1 10. (New) The method of claim 1, wherein:
2 said step of inhibiting the FIFO device from changing state of
3 the FIFO output signal, thereby inhibiting further burst transfers
4 includes
5 the processor device supplying to the FIFO device an end
6 of burst signal upon completion of a burst transfer, and
7 inhibiting the FIFO device from changing state of the
8 FIFO output signal until receipt of said end of burst signal.

1 11. (New) The method of claim 1, wherein:
2 said step of inhibiting the FIFO device from changing state of
3 the FIFO output signal, thereby inhibiting further burst transfers
4 includes
5 the FIFO device counting a predetermined number of cycles
6 corresponding to a burst transfer size, and

7 inhibiting the FIFO device from changing state of the
8 FIFO output signal until completion of counting the
9 predetermined number of cycles.